Remarks

Applicant has amended claims 1, 3 to 5, canceled claims 2 and 17, and added claims 18 to 27.

§ 102 Rejections

The Examiner rejected claims 1 to 17 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,026,464 ("Cohen"). Applicant has amended claim 1 to include the limitations of claim 2. Amended claim 1 now recites:

> 1. A node controller for a data storage system having at least one node for providing access to a data storage facility, the node controller distinct from a computer-memory complex of the node, the node controller providing overall control for transferring data through the node, wherein the node controller comprises a logic engine operable to perform a logic operation on data from at least one data source in the data storage system.

Amended claim 1 (emphasis added). This is supported in the Specification, which states:

> Logic engines 56 in node controller 12 can operate (e.g., perform an XOR operation) on data from up to thirteen sources (in local cluster memory 20 or PCI buses 36) and write the result into a destination (in either local cluster memory 20, one of the two PCI buses 36, or one of communication paths 16). The sources, destination, length, and operation type and flags are programmed in one or more logic control blocks (LCBs) stored in respective command queues 58.

Specification, p. 15, line 20 to p. 16, line 1. The XOR operation, which is recited in dependent claims, is particular relevant to the present invention because it is used to calculate parity data in a RAID write and also to reconstruct lost data using parity data in a RAID system.

The Examiner rejected original claims 1 and 2 for the following reasons.

> Regarding claim 1, Cohen discloses a node controller (Figure 1, 18) for a data storage system having at least one node for providing access to a data storage facility (Figure 1, 30), the node controller distinct form a computer-memory complex, the node controller providing overall control for transferring data through the node.
>
> Regarding claim 2, Cohen discloses a node controller comprising a logic engine operable to perform a logic operation on data form at least one data source in the data storage system (Column 6, Lines 5-7).

12/24/03 Office Action, p. 2. Applicant respectfully traverses.

Cohen does not disclose "a logic engine operable to perform a logic operation on data from at least one data source in the data storage system" as recited in claim 1. The Examiner cites col. 6, lines 5 to 7 of Cohen for disclosing such a logic engine. The entire paragraph containing lines 5 to 7 discloses:

> The memory bus monitor 60 monitors all bus commands, control signals, and the bank selection bits transmitted from each memory controller 18. The bank state memory 54 contains an entry for each memory bank 70 within the memory system 20 that indicates the current state of the memory bank (BUSY or IDLE) and counters indicating the "activate" status and "precharge" status. The status of memory bus monitor 60 signals to the master controller 58 changes to initiate pending memory transactions. The different circuits in the memory controller 18 are implemented in combinational logic and registers.

Cohen, col. 5, line 64 to col. 6, line 7. Although this paragraph discloses that memory controller 18 is implemented with combination logic, it does not disclose that memory controller 18 performs a logic operation on data from one or more data sources in a data storage system. Cohen only discloses a scheme in which multiple memory controllers 18 arbitrate for writing to memory bank 70.

> The memory controller 18 receives access requests from the connected processing device(s), and then checks the state of the addressed memory bank 70. For example, memory controller 18A reviews requests from CPU 14. If that targeted memory bank 70 is idle, the memory controller 18 arbitrates for the memory bus 22 and "activates" that memory bank 70. Each memory controller 18 sees the activate command and marks that memory bank 70 as busy. When the data for the activated memory bank 70 is ready for access, the memory controller 18 arbitrates a second time for a data bus transaction. When granted the data bus, the memory controller 18 bursts the data from the memory subsystem 20 for a read or writes the data into the memory subsystem 20. When the data bus transaction is completed, each memory controller 18 marks that memory bank 70 idle.
>
> Each memory controller 18 queues accesses to memory banks 70 that are currently busy, and completes the queued accesses when the memory bank 70 is free. If other memory requests are received for free memory banks, after the queued accesses, the memory controller 18 processes the requests for the free memory banks, out-of-order. Processing memory requests out of order increases memory throughput since one busy memory bank will not delay access to other available memory banks.

Cohen, col. 3, lines 47 to co. 4, line 4. Cohen does not mention performing any logic functions from one or more data sources in a data storage system. Accordingly, amended claim 1 is patentable over Cohen.

Applicant has canceled claim 2, thereby rendering its rejection moot.

Claims 3 to 8 depend from claim 1 and are patentable over Cohen for at least the same reasons as claim 1.

Independent claim 9 includes a limitation of "a logic engine operable to perform a logic operation" and is therefore patentable over Cohen for at least the same reasons as claim 1.

Claims 10 to 16 depend from claim 9 and are patentable for at least the same reasons as claim 9.

Applicant has canceled claim 17, thereby rendering its rejection moot.

New claims

Applicant has added new claims 18 to 27.

Independent claim 18 includes a limitation on the "logic engine performs the logic operation" and is therefore patentable over Cohen for at least the same reasons as claim 1.

Claims 19 to 27 depend from claim 18 and are patentable for at least the same reasons as claim 18.

In summary, claims 1 to 17 were pending in the above-identified application when last examined. This Response amends claims 1 and 3 to 5, cancels claims 2 and 17, and adds claims 18 to 27. For the above reasons, Applicant respectfully requests the Examiner with withdraw the claim rejections and allow claims 1, 3 to 16, and 18 to 25. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

Certification of Facsimile Transmission

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature _____ Date March 18, 2004

Respectfully submitted,

David C. Hsia
Attorney for Applicant(s)
Reg. No. 46,235